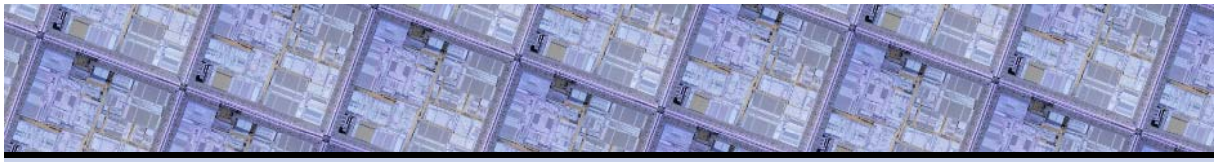


The Frontiers of Robust Circuit Design
in Sub-28nm Process Technologies

Jim Dodrill
ARM

ISQED Symposium 2015

ARM® ARTISAN® Physical IP

ISQED Symposium 2015

"The conventional wisdom that led to our success in the past will no longer work in the future."

Cliff Hou, VP R&D, TSMC, at DAC 2014

Agenda

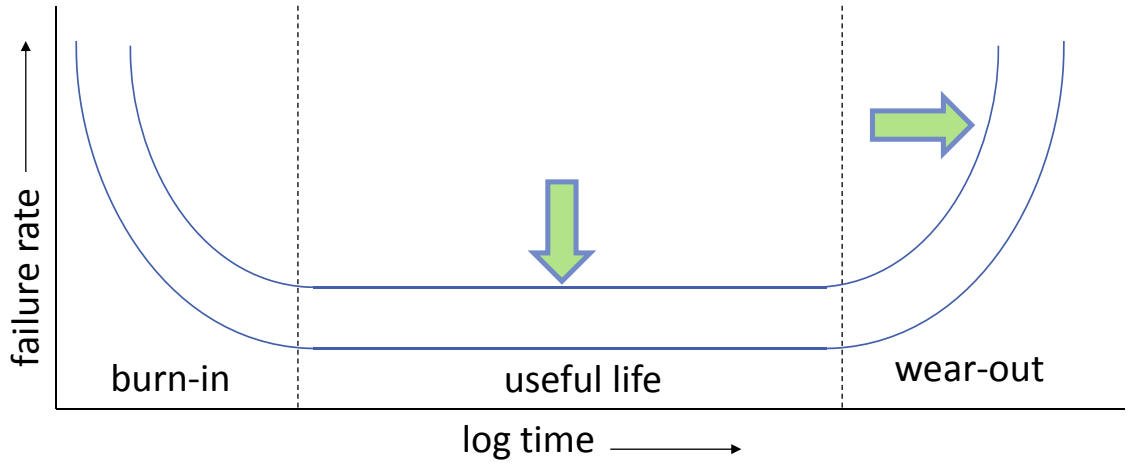
- The Cost of Design Margins
- FinFET Changes the Landscape
- Variation
  - Process, Voltage, and Temperature
  - Location and Layout Dependent Effects
- Random Failures
  - Radiation, Synchronization, and Noise
- Aging
  - BTI, HCI, EM, and TDDB
- Putting it All Together

Focus

- Focus is on SoC implementation aspects
  - Assume foundry and IP partners have done their best to offer reliable products
- For each failure mechanism:
  - Introduce the physical background
  - Compare planar vs. FinFET
  - Offer practical design advice

Device Lifetime

- Testing
  - defects
  - variation
- Random Failures
  - soft errors
  - synchronization
  - noise
- Aging
  - BTI, HCI
  - EM, TDDB



The Heart of the Matter…

"At the heart of reliability engineering is the fact that there is a distribution of lifetimes for each failure mechanism. With low failure rate requirements we are interested in the early time-range of the failure time distributions. There has been an increase in process variability with scaling (e.g., distribution of dopant atoms, CMP variations, and line-edge roughness). At the same time the size of a critical defect decreases with scaling. These trends will translate into an increased time spread of the failure distributions and, thus, a decreasing time to first failure."

ITRS 2013, Process Integration, Devices, and Structures

Tactics

- Margining
- Thermal Management
- Dynamic Voltage and Frequency Scaling (DVFS)
  - In-situ monitors
  - Adaptive Supply Voltage (ADV) or Back-Bias (ABB)
- Redundant Components
  - Error Detection and/or Correction
  - Time Multiplexing (Resource or Task Allocation)
  - Cannibalization (Resource Sharing)

The Cost of Design Margins

Moore's Law
Dark Silicon
Margin Cost

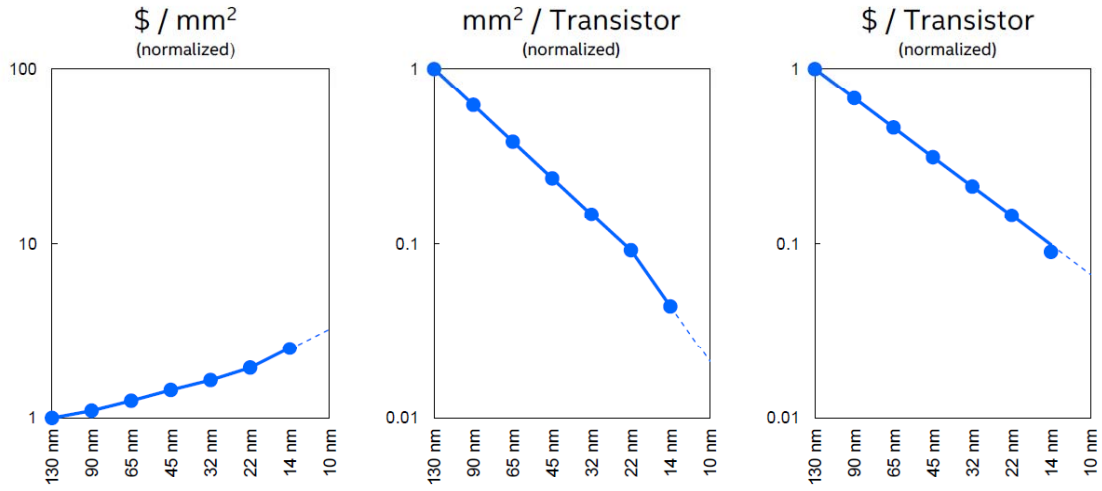
isQED
Symposium 2015

"Traditional VLSI design bypasses the analysis and optimization of such non-uniform, dynamic network by approximating the problem into optimization of uniform static network with certain guard band."

Muhammad Alam,
"Reliability- and process-variation aware design of integrated circuits"
2008 Elsevier Ltd.

Moore's Law is Still Alive

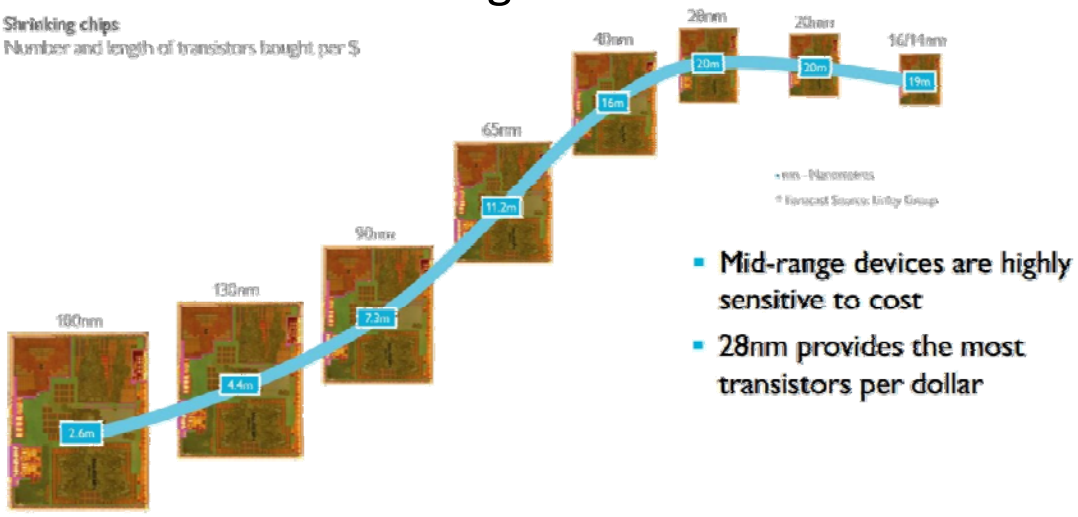
- The cost per transistor continues to reduce
  - Or does it?



Source: Bill Holt (Intel), *"Intel Investor Meeting,"* (2014)

Another View…

- Lower yield will drive costs up in at 20nm and smaller while competition will drive costs down at 28nm and larger.



The Dark Silicon Apocalypse

"Where once we would spend exponentially increasing amounts of silicon area to buy performance, now, we will spend exponentially increasing amounts of silicon area to buy energy efficiency."

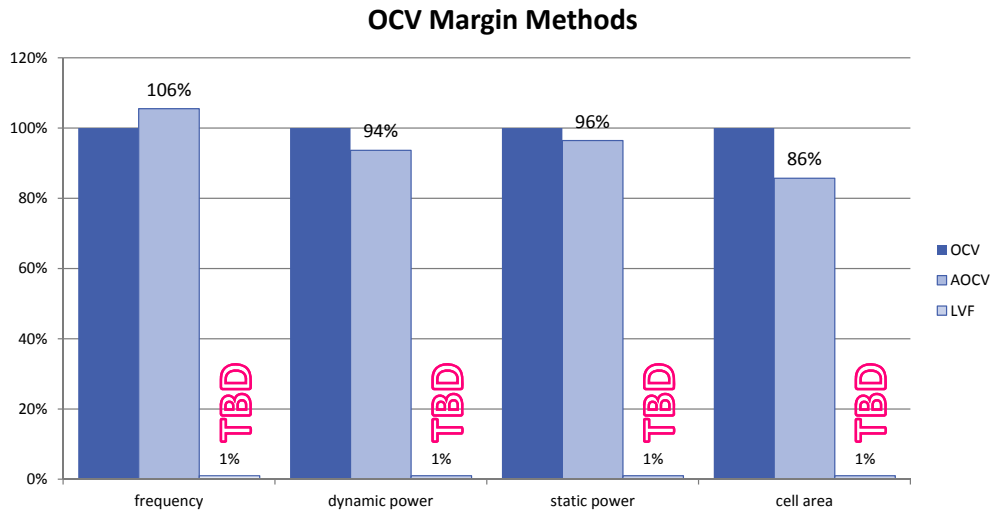
Michael B. Taylor, "*Is Dark Silicon Useful? Harnessing the Four Horsemen of the Coming Dark Silicon Apocalypse*," ACM (2012)

Will increasing amounts of silicon area be used to buy reliability?

Of course!

Timing Margins

- More accurate modeling of timing variation results in more efficient implementations

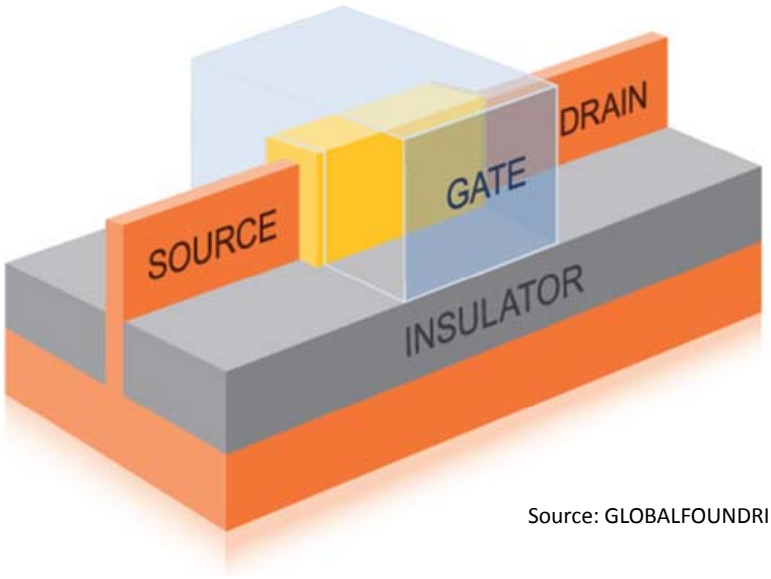


FinFETs Change the Landscape

Planar vs. FinFET

Multi-patterned Interconnect

Introducing the FinFET

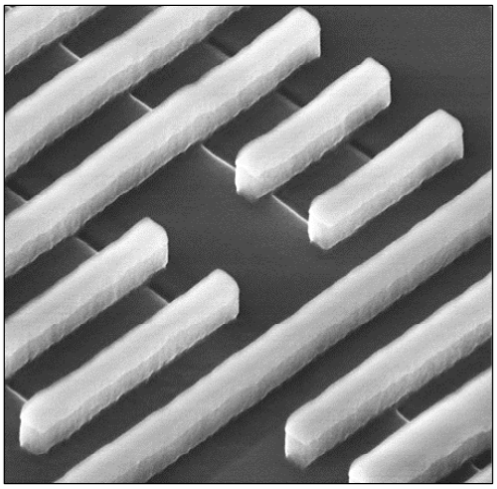


Source: GLOBALFOUNDRIES

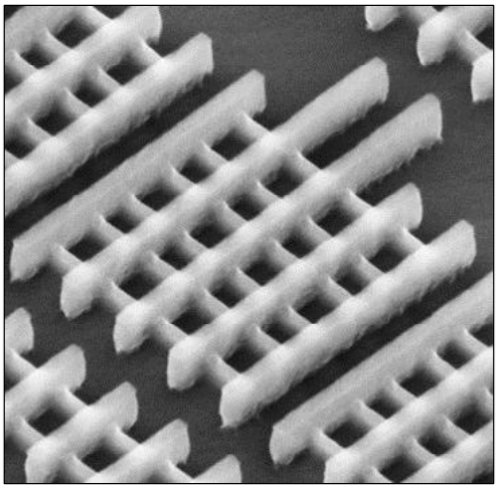
Planar vs. FinFET

ISQED Symposium 2015

32 nm Planar Transistors



22 nm Tri-Gate Transistors

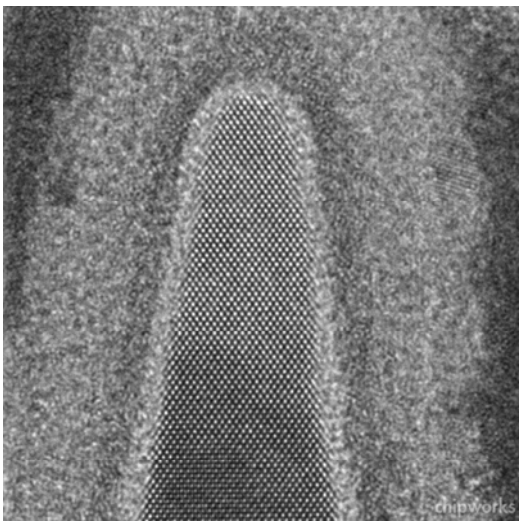


Source: Mark Bohr , et al. (Intel) (2011)

Fins are Very Thin

ISQED Symposium 2015

- This is a TEM image of the Intel 22nm Fin
- At 14nm, Fins will be about 20 atoms wide



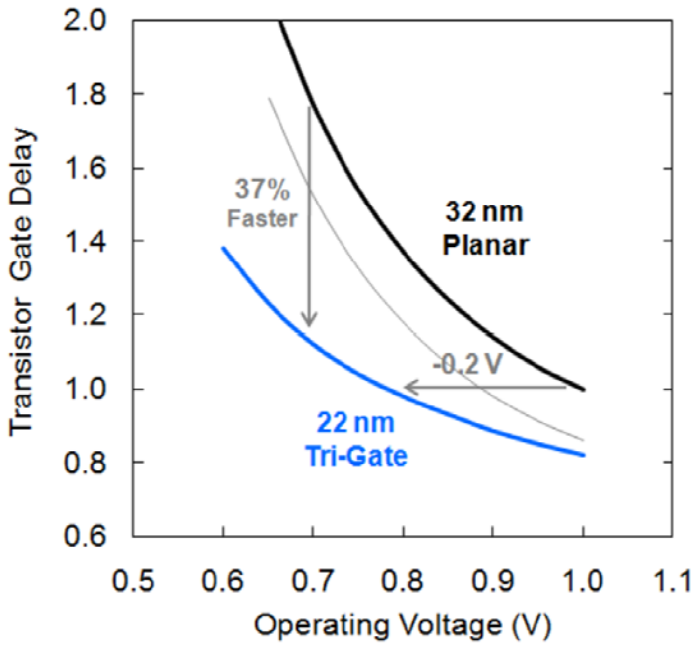
Chipworks (2012)

The Future…

N 20	N 20 / N 14	N10	N 20 / N 7	N 7 / N 5	N 5 / N 3.5
Bulk CMOS: Complementary Metal Oxide Semiconductor	**SOI:** Partially depleted Silicon on insulator	**SOI:** Fully depleted Silicon on insulator	**Bulk FinFet :** fin field effect transistor	**SOI FinFet :** silicon on insulator fin field effect transistor, III-V	Gate-all-around transistor

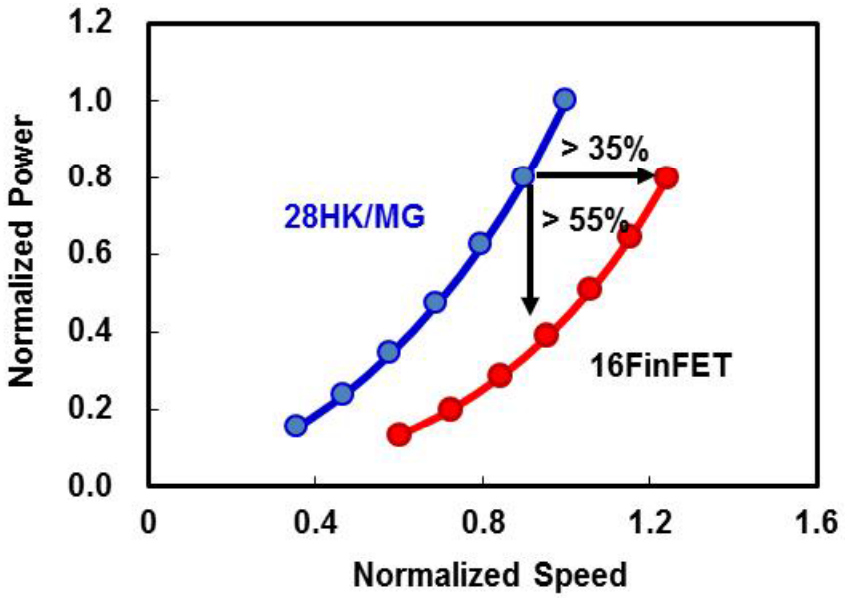
Source: Martin van den Brink, "*Many ways to shrink: The right moves to 10 nanometer and beyond*," AMSL (2014)

Delay vs. Voltage



Source: Mark Bohr , et al. (Intel) (2011)

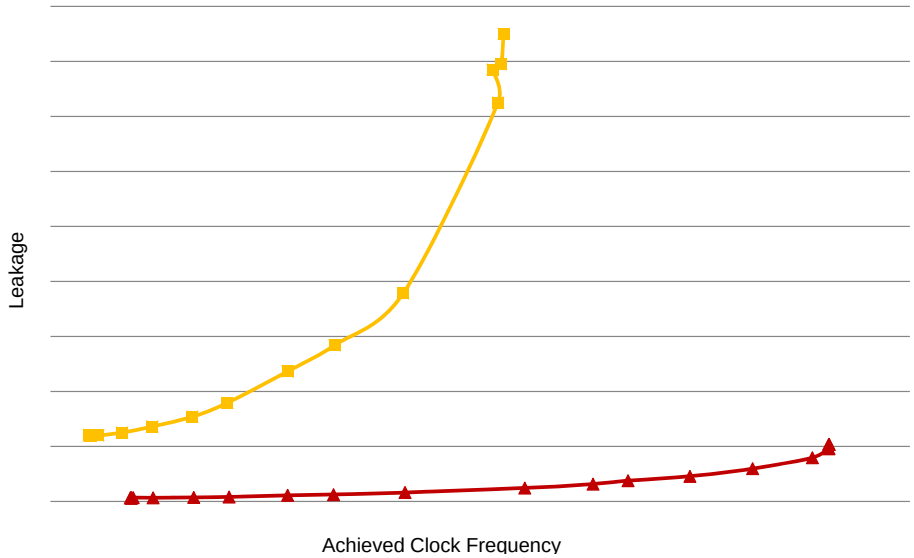
Power vs. Speed



Source: Shien-Yang Wu, et al. (TSMC), IEDM (2013)

Leakage vs. Achieved Frequency

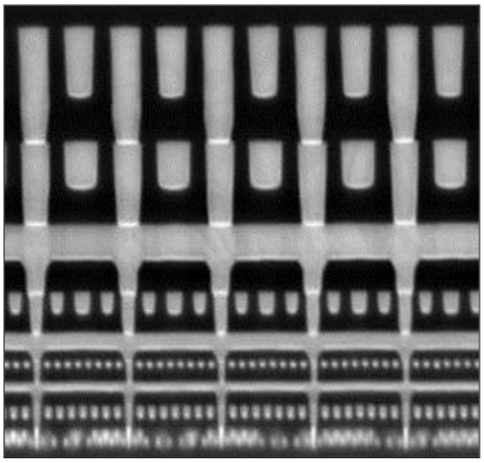
- Leakage reduction from FinFET is significant



Source: Leah Schuth, (ARM) (2014)

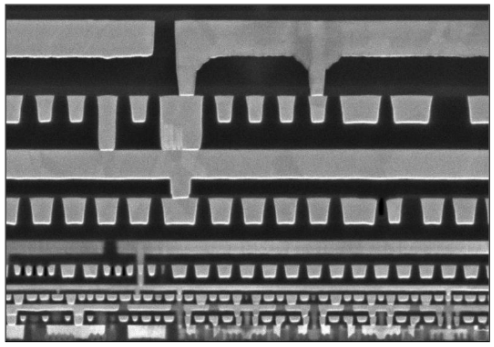
Interconnect

22 nm Process



80 nm minimum pitch

14 nm Process

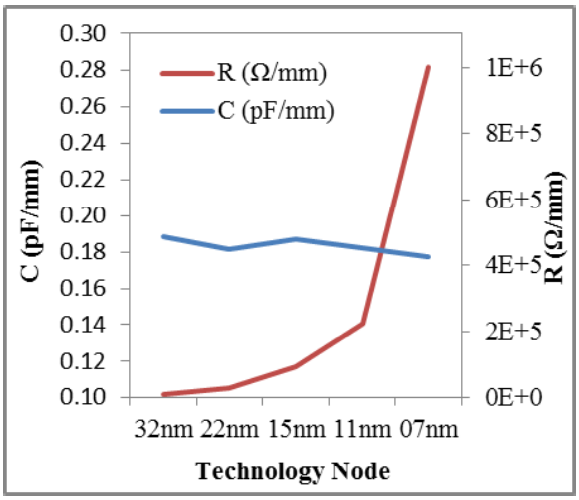


52 nm (0.65x) minimum pitch

Source: S. Natarajan, et al. (Intel), IEDM (2014)

Wire Resistance

- The RC time constant of wires is increasing substantially as line widths reduce

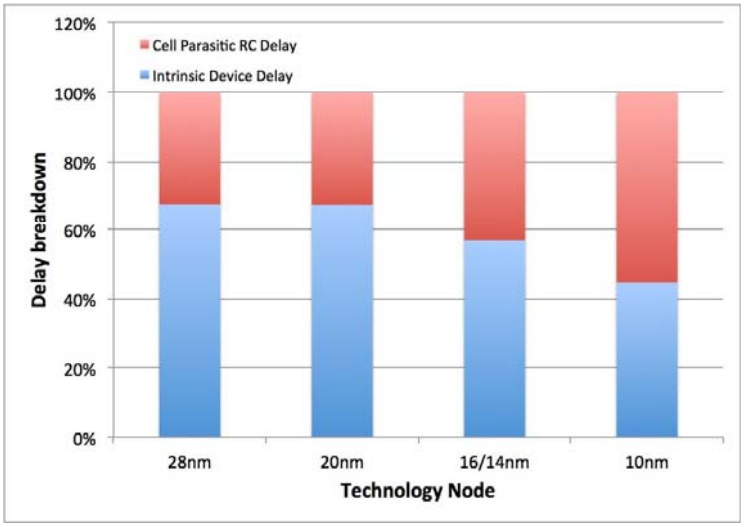


Source: Serkan Kincal, et al., "*RC* Performance Evaluation of Interconnect Architecture Options Beyond the 10-nm Logic Node," IEEE (2014)

Cell vs. Wire Delay

ISQED Symposium 2015

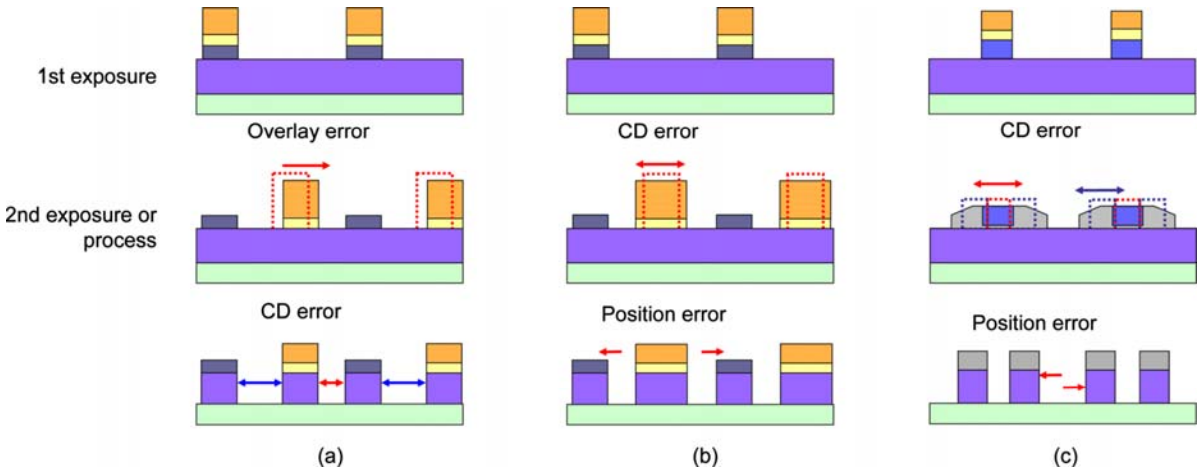
- Wire delay is becoming as big as cell delay
  - We've heard this for years, but its real now



Source: Greg Yeric (ARM), "Design, Technology and Yield in the Post-Moore Era," ITC (2014)

Double Patterning

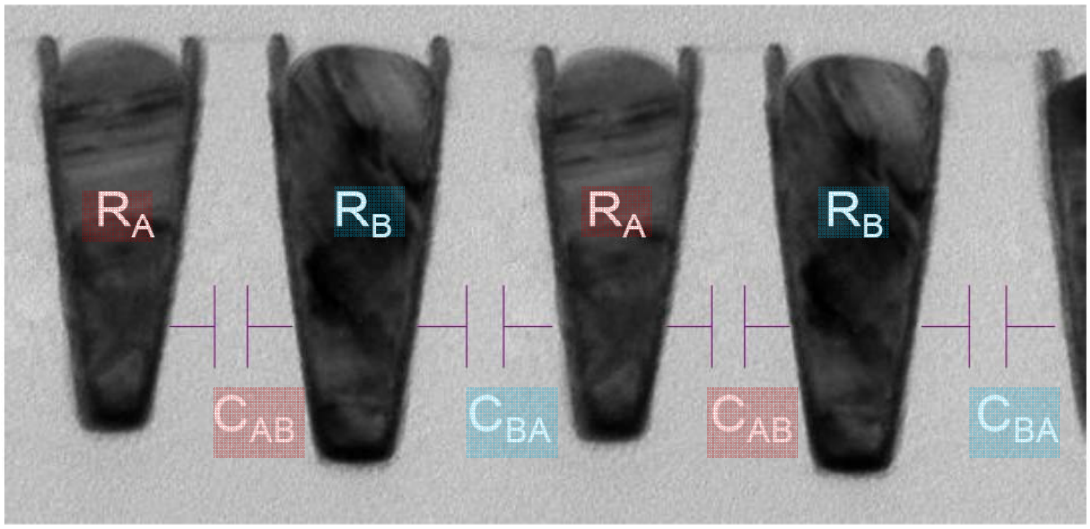
ISQED Symposium 2015



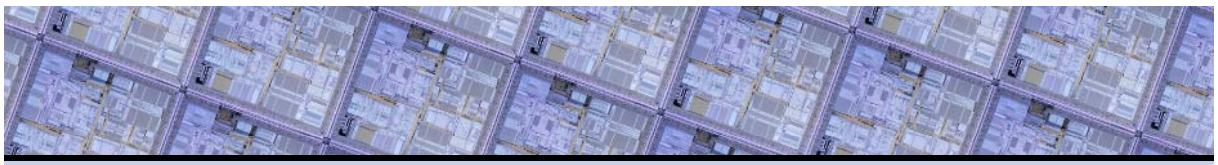
Source: Andrew J. Hazelton, et al. "*Double-patterning requirements for optical lithography and prospects for optical extension without double patterning,*" *J. Micro/Nanolith. MEMS MOEMS (2009)*

RC Variation

- Note the wire thickness and spacing differences in the two metal patterns, A & B



Source: ITRS 2013 EDITION: INTERCONNECT

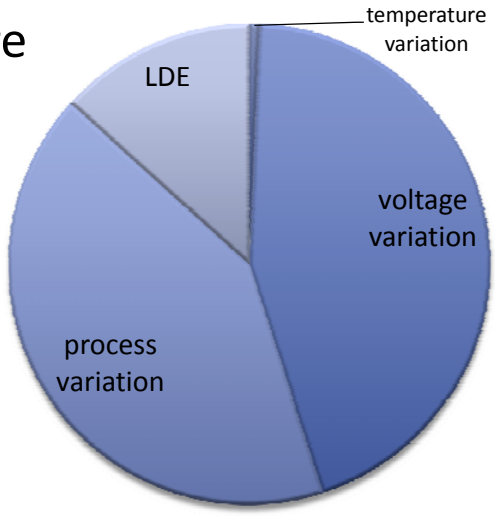


On-Chip Variation

Process, Voltage & Temperature Variation
Layout Dependent Effects
OCV Modelling

Sources of Variation

- Process (transistor and wire)
- Voltage
- Layout Dependent Effects (LDE)
- Temperature



Variation: Planar vs. FinFET

- Single fin FinFETs are not used due to high variation

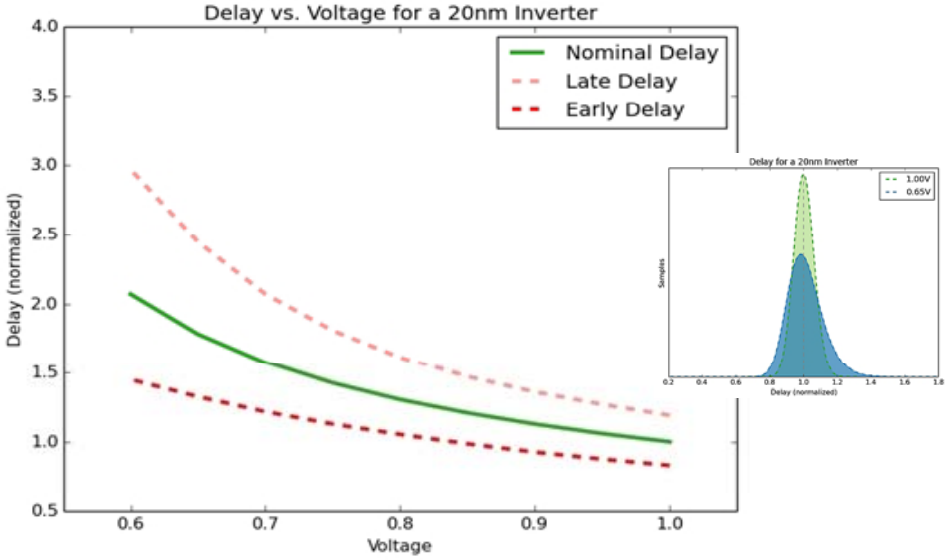
Source	Planar	FinFET
Random Dopant	✓	✓(less)
Line Edge Roughness	✓	✓
Gate Edge Roughness	✓	✓
Gate Granularity	✓	✓
Fin Edge Roughness		✓
Fin Height		✓
Fin Shape		✓

Source: Greg Yeric (ARM), "Design, Technology and Yield in the Post-Moore Era," ITC (2014)

Variation vs. Voltage

ISQED Symposium 2015

- Delay and variation increase as voltage decreases

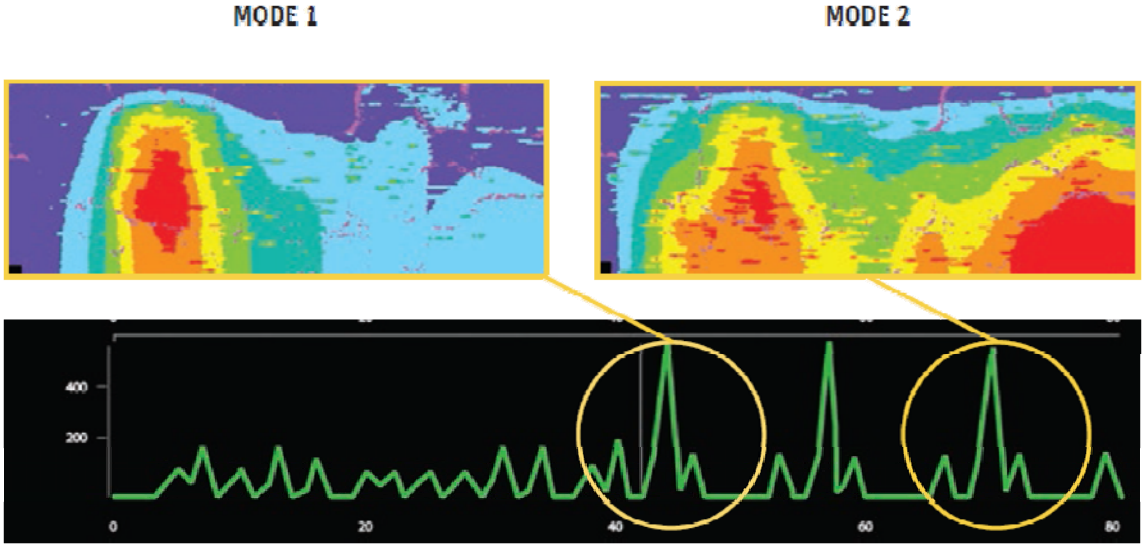


Source: Isadore Katz, CLK DA (2014)

Voltage Variation

ISQED Symposium 2015

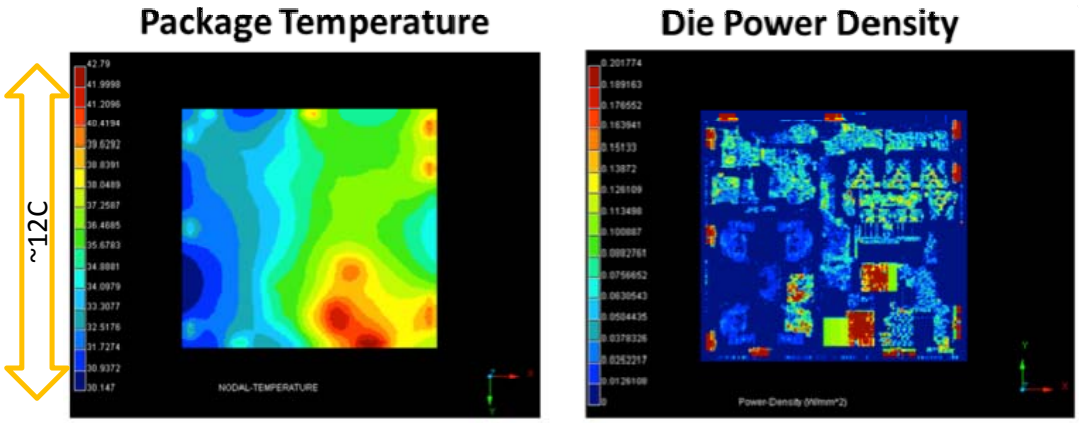
- Chip dynamic voltage drop based on two different operating modes



A. Shanmugavel, Ansys Inc. (2013)

Temperature Variation

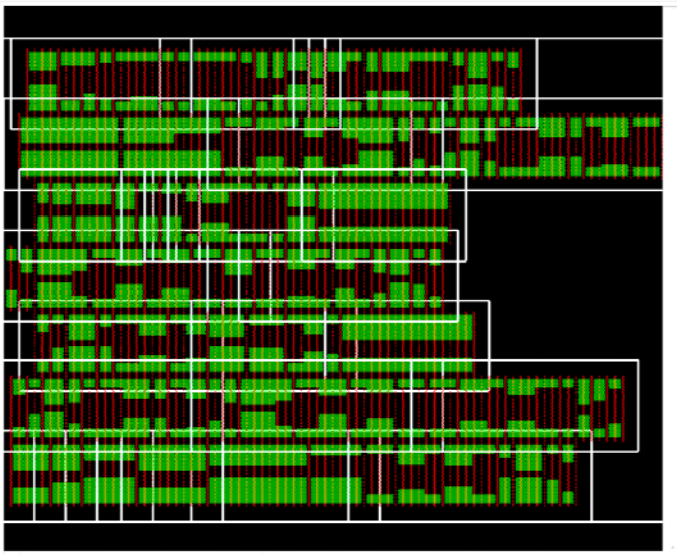
- Thermal conduction from the channel
  - planar transistors: tends toward the substrate
  - finFET transistors: tends toward the metal



A. Shanmugavel, Ansys Inc. (2013)

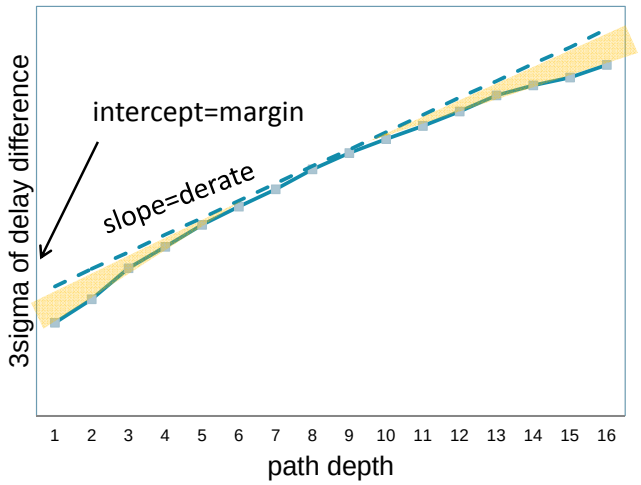
Layout Dependent Effects

- Non-uniformities in the surrounding context of a transistor adds to delay variation



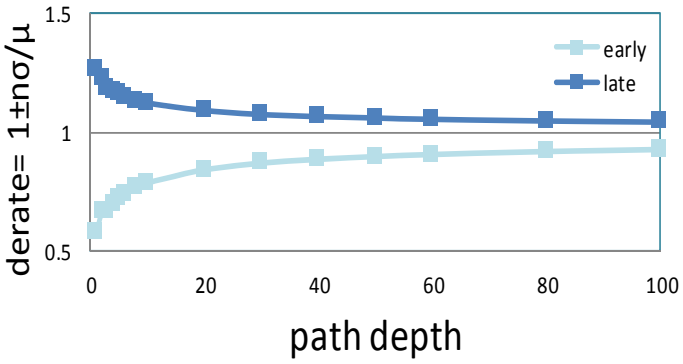
OCV Modeling

- Traditional OCV
  - Percentage derate applied to clock paths
  - Plus a fixed margin added to the clock uncertainty



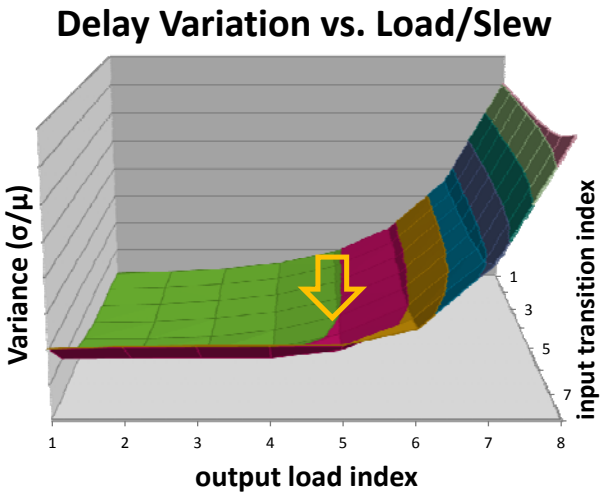
AOCV Modeling

- Advanced OCV (AOCV)
  - Tables of derate values for cells and nets indexed by path depth
  - These tables are called Stage-Based OCV (SB-OCV)
  - May include location-based (LOCV) derate tables



Stage Based-OCV Limitation

- SB-OCV is limited to:
  - One timing arc per cell
  - One load/slew point



OCV Modeling

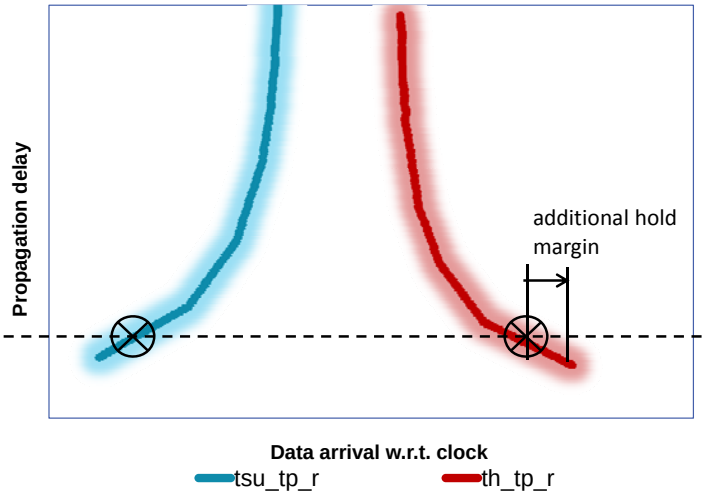
- Liberty Variance Format (LVF)
  - Table of sigma values for cell delay, transition time, and constraints in the Liberty model
  - Derates are calculated by the timing engine based on N*sigma and path depth

	LOAD				
SLEW	σ	σ	σ	σ	σ
	σ	σ	σ	σ	σ
	σ	σ	σ	σ	σ
	σ	σ	σ	σ	σ
	σ	σ	σ	σ	σ

Statistical Constraint Margins

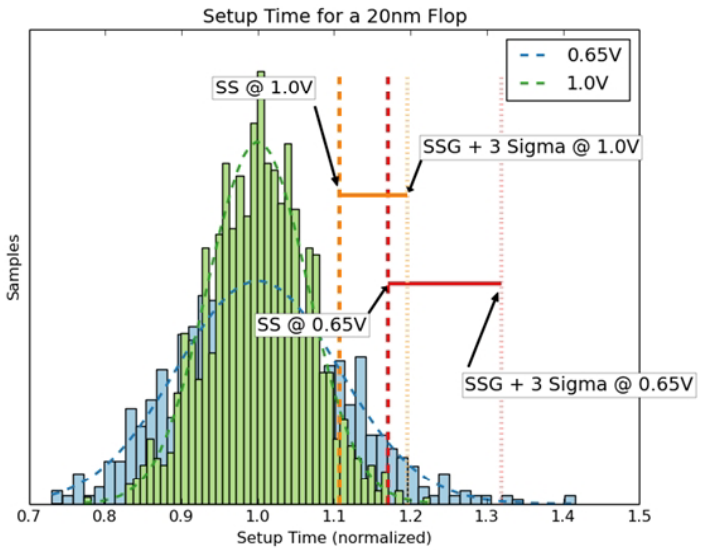
- Timing Constraints also have variation
  - Usually only hold and removal constraints are margined

Setup and hold are defined by a specified increase in CK->Q



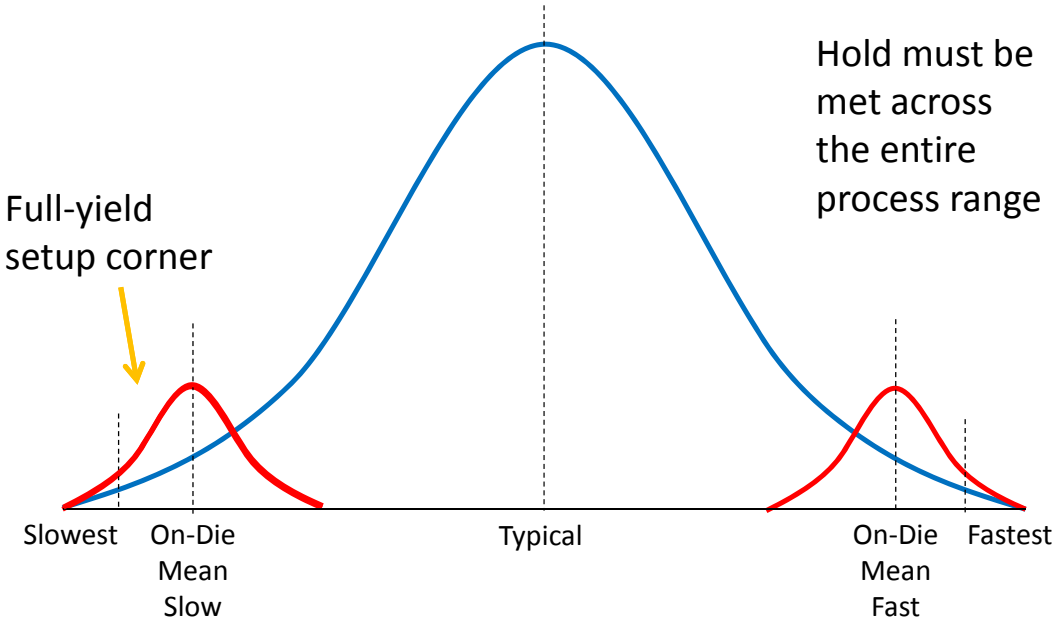
Constraint Margins vs. Voltage

- The variation of also constraints increases as voltage decreases



Source: Isadore Katz, CLK DA (2014)

PVT Corners



Determining N*sigma

- LVF allows users to choose N*sigma
  - Native die yield should dominate, not timing yield

Step	Example	
	Yield	Failure Rate
Estimate manufacturing yield	95%	5/100
Chose a timing yield target that is better	97%	3/100
Estimate the number of near-critical hold paths	50K	2/100K
multiply	99.99994%	6/10M
Derive sigma	about 5σ	

"Statisticians, like artists, have the bad habit of falling in love with their models."

-- George Box

Practical Advice

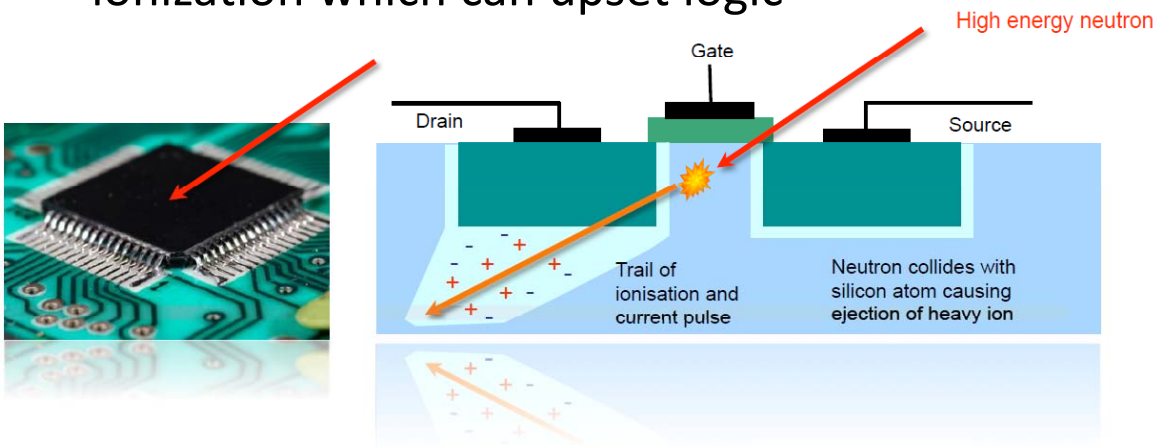
- Use the latest, most accurate variation models available
  - Consult your foundry and IP provider for guidance
- Be sure to account for non-obvious variation
  - Layout Dependent Effects
  - Wire Variation
- Consider the cost of design margins
  - Yield loss vs. power, area, and design schedule
  - **Prioritize good hold margins**

Random Failures

Soft Error Rate (SER)
Synchronization
Random Telegraph Noise (RTN)

The Neutron Strike

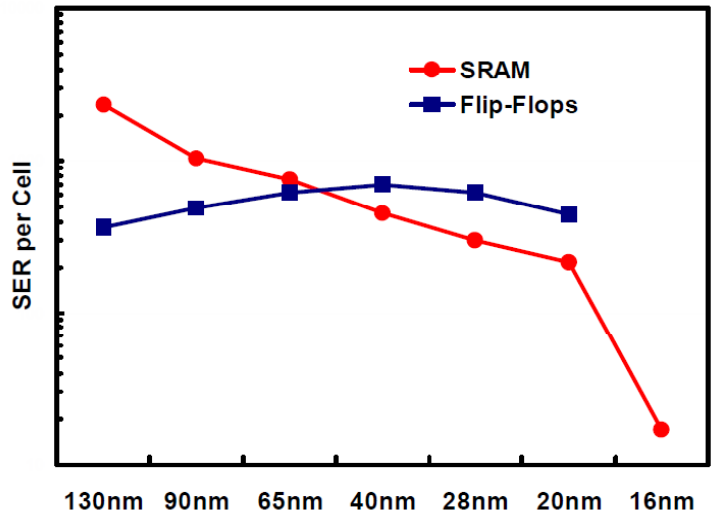
- Cosmic radiation includes alpha particles and high energy neutrons that can create ionization which can upset logic



Source: Christopher Frost, *"How Alien Invaders Can Change Governments,"* ISIS (2014)

SER of Planar vs. FinFET

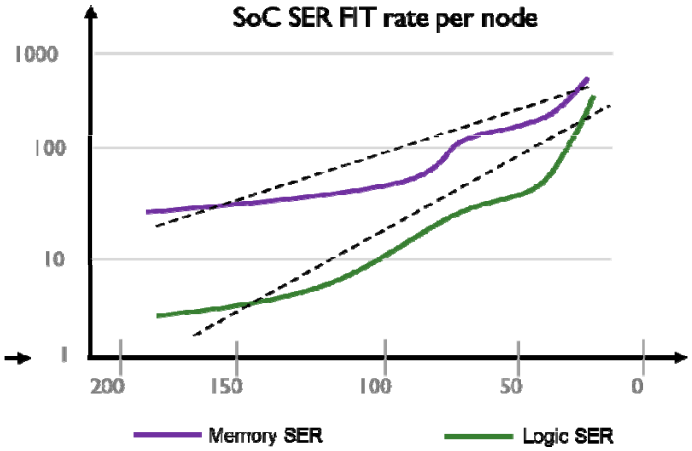
- The trend is for improvement in SER
  - FinFET has 3X-10X lower SER than planar



Anthony S. Oates (TSMC), *"Will Reliability Limit Moore's Law?,"* IEDM (2014)

SER of Systems

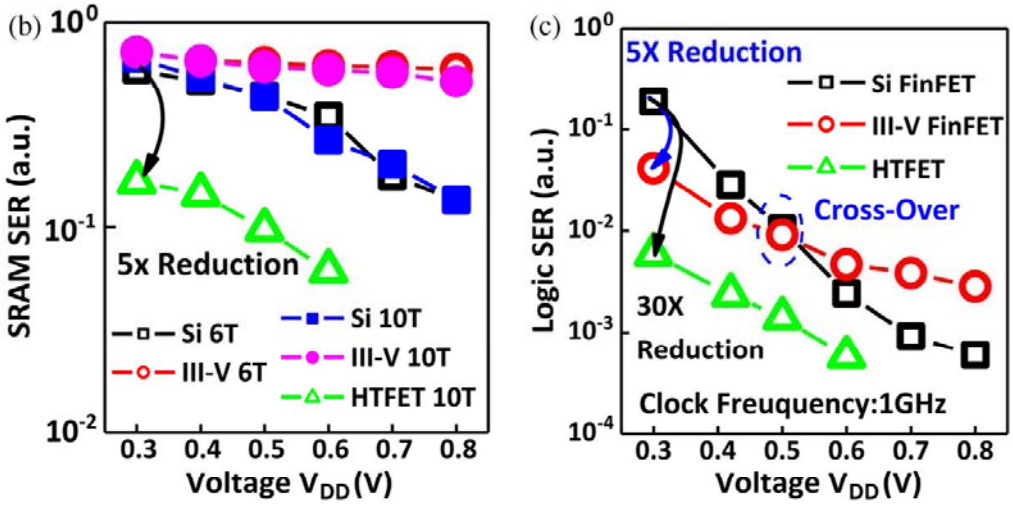
- While the SER of individual state elements is improving, overall chip SER is not
  - Flip-flops dominate in systems with ECC



Source: Vikas Chandra, *"Cross layer resilience in real world,"* DATE (2014)

SER vs. Voltage in FinFET

- SER increases as voltage decreases
  - Various FinFET technologies can improve SER



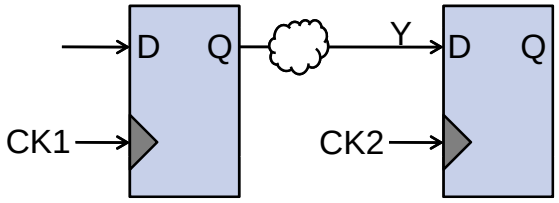
Source: Huichu Liu, et al., *"Soft-Error Performance Evaluation on Emerging Low Power Devices,"* IEEE (2014)

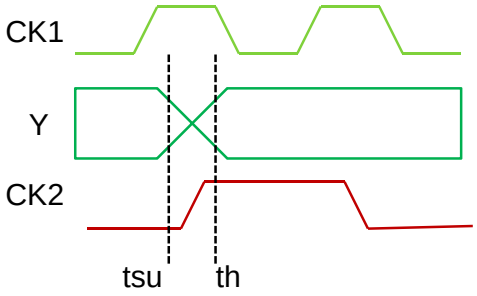
Practical Advice

- Acquire FIT rate estimates from foundries and IP providers
  - Consider the lowest operating voltage domain
- Determine which state elements contribute the most to the probability of program failure
  - The "Architectural Vulnerability Factor" (AVF)
  - Harden those state elements
- Use appropriate error detection and correction

Clock domain crossing

- Synchronizers are used when data crosses between two asynchronous clock domains.
  - That means data can change during the window between the setup and hold constraints.

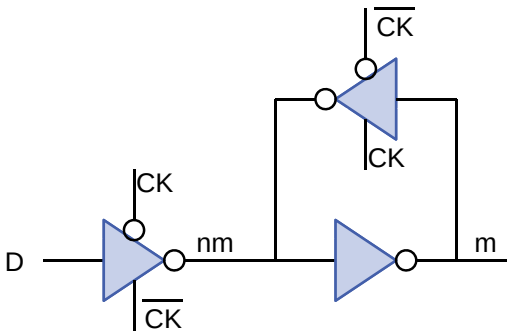


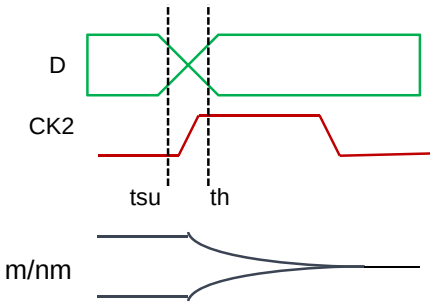


CK1 and CK2 are asynchronous

Metastability

- When setup and hold constraints are violated, the signals inside the receiving flip-flop can fail to resolve within a clock period





m fails to resolve to '1' or '0'

MTBF for Synchronizers

ISQED Symposium 2015

$$MTBF = \frac{e^{T_s/\tau}}{T_W \cdot fd \cdot fc \cdot n}$$

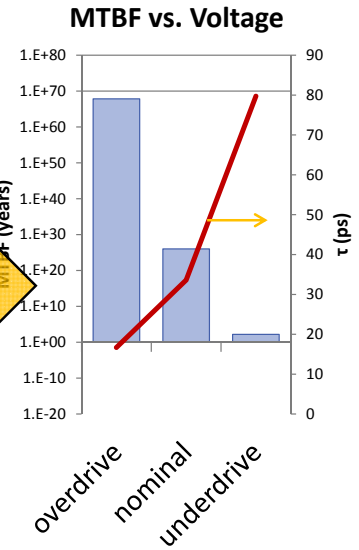
T_S	is the resolution time, which is approximately the clock period
τ	is the resolution time constant, a function of the latch design and PVT corner
T_W	is the time window, also a function of the latch design and PVT
f_d	is the data frequency
f_c	is the clock frequency
n	is the number of synchronizers in the entire system

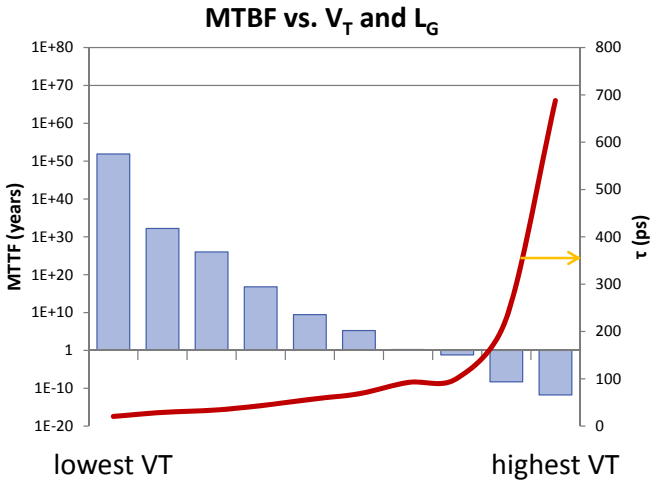
MTBF vs. Voltage

ISQED Symposium 2015

- MTBF reduces as voltage decreases
  - MTBF also decreases as the period decreases
  - VT choice is critical

The universe is $1.38*10^{10}$ years old



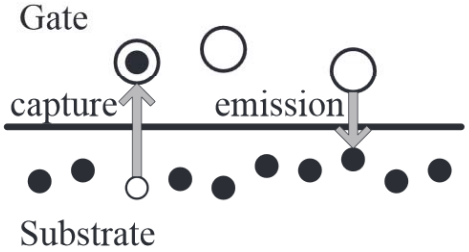


Practical Advice

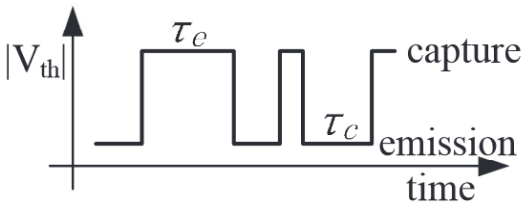
- Use specially constructed synchronizer cells
  - One cell, N-stages deep
  - Choose the lowest V_T and shortest L_G available
- Obtain the necessary MTBF parameters for your synchronizers
  - Use the model for an average transistor on a slow die
  - Calculate the MTBF at each voltage and frequency combination
  - Account for the total number of synchronizers in the computing system

Random Telegraph Noise

- Random Telegraph Noise (RTN) is caused by the capture and emission of carriers at traps (defects) in the oxide boundary



(a) Capture/emission of traps.

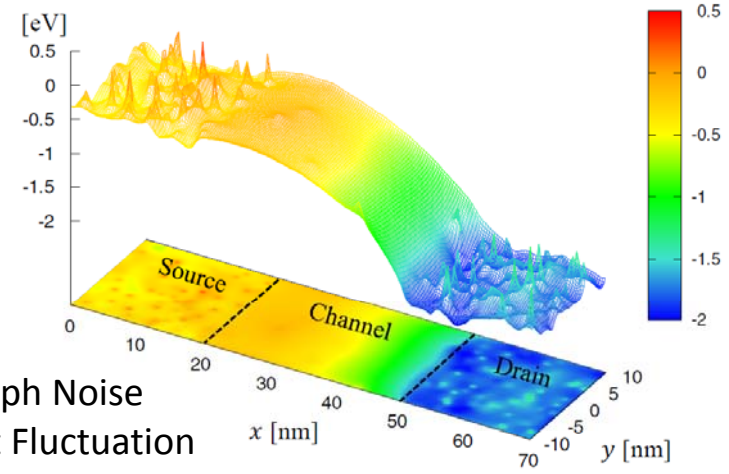


(b) V_{th} fluctuation.

Source: Xiaoming Chen, et al., *"Statistical Analysis of Random Telegraph Noise in Digital Circuits,"* IEEE (2014)

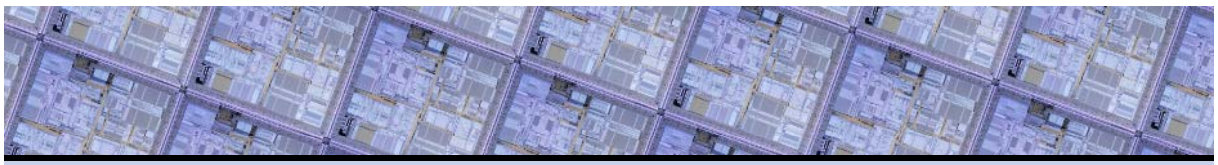
Random Telegraph Noise

- *"The static variability of the source-induced RDF is found to overwhelm the dynamic on-current fluctuation due to RTN."*



RTN = Random Telegraph Noise
RDF = Random Dopant Fluctuation

Source: Akito Suzuki, et al, *"Source-induced RDF Overwhelms RTN in Nanowire Transistor: Statistical Analysis with Full Device EMC/MD Simulation Accelerated by GPU Computing,"* IEEE (2014)

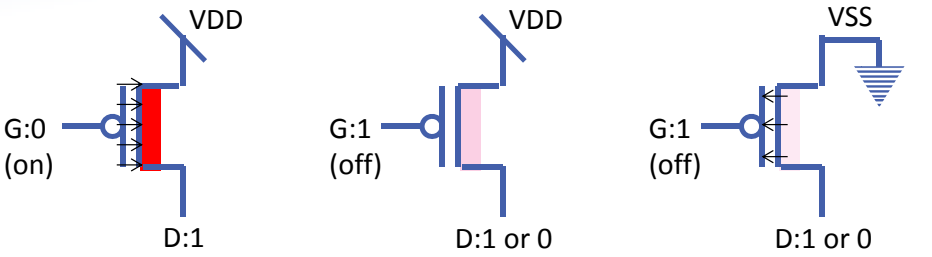


Aging

BTI: Bias Temperature Instability
HCI: Hot Carrier Injection
EM: Electro-migration
TDDB: Temperature Dependent Dielectric Breakdown

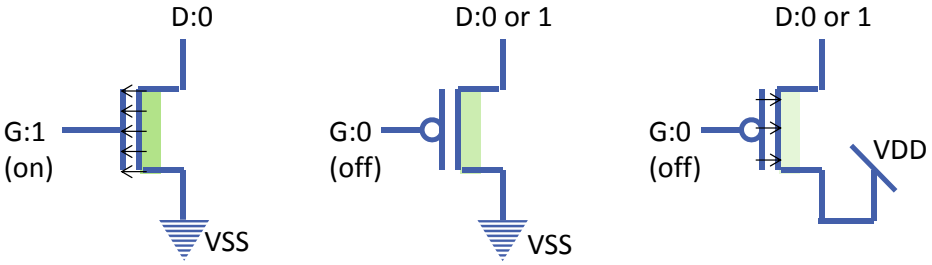
BTI: Stress and Recovery

PMOS: Negative Bias Temperature Instability (NBTI)



Stress | **Natural Recovery** | **Proactive Recovery**

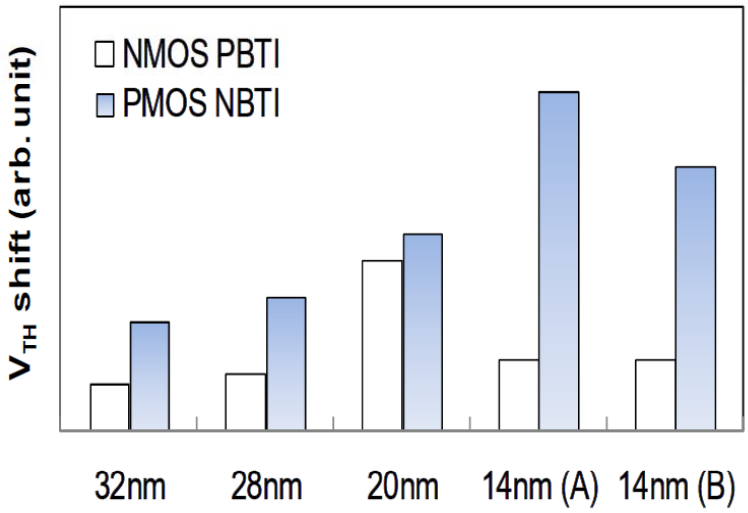
NMOS: Positive Bias Temperature Instability (PBTI)



Based on: Lin Li, *"Improving the Reliability of Microprocessors Under BTI and TDDB Degradations,"* University of Pittsburgh (2014)

BTI: Planar vs. FinFET

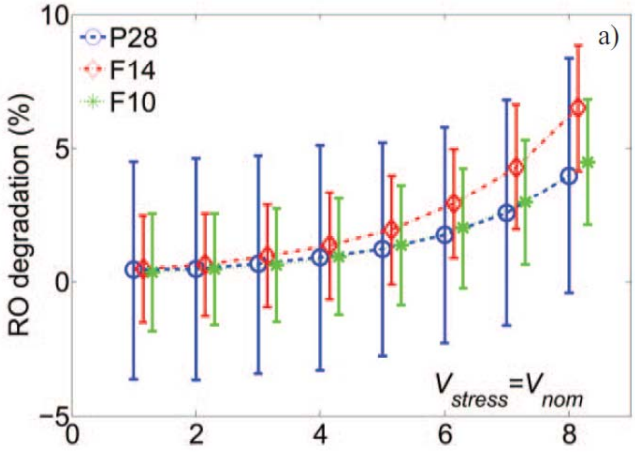
- The V_T shift due to PBTI is lower, and due to NBTI is higher for FinFET



Kyong Taek Lee, (Samsung) IEEE (2013)

BTI: Ring Oscillator Degradation

- V_T shifts due to BTI lead to larger propagation delay

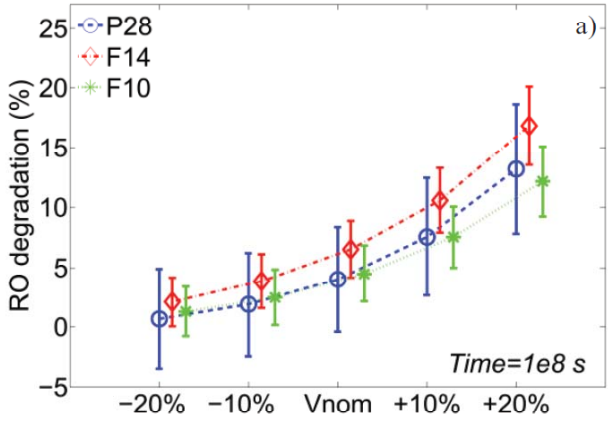


Source: Halil Kükner, et al., *"Scaling of BTI reliability in presence of Time-zero Variability,"* IEEE (2014)

BTI vs. Voltage

- At higher voltage, delay degradation is more

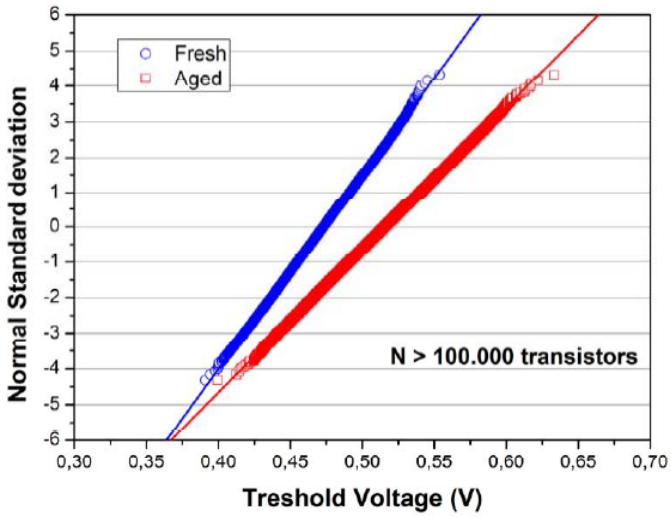
$$\Delta V_{th} = Ae^{\left(\frac{-E_a}{kT}\right)}e^{(\gamma V_{gs})}t^n$$



Source: Halil Kükner, et al., *"Scaling of BTI reliability in presence of Time-zero Variability,"* IEEE (2014)

BTI and Variation

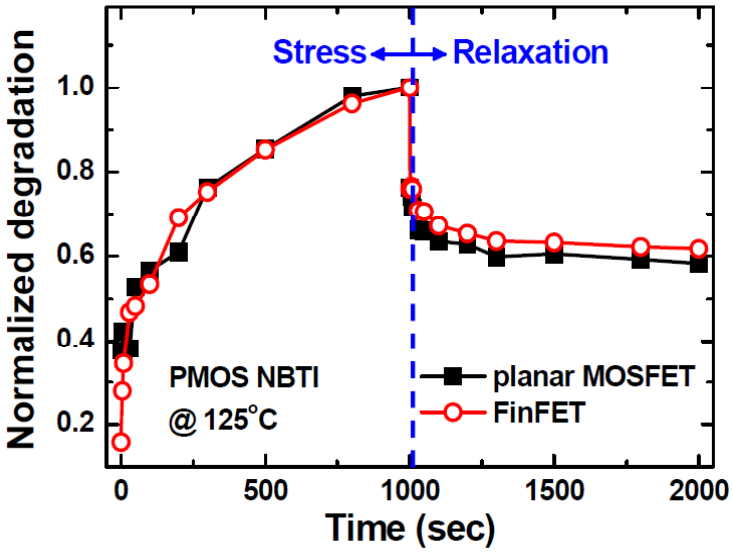
- Process variation remains a normal distribution after aging



D. Angot, et. al. , IEDM (2013)

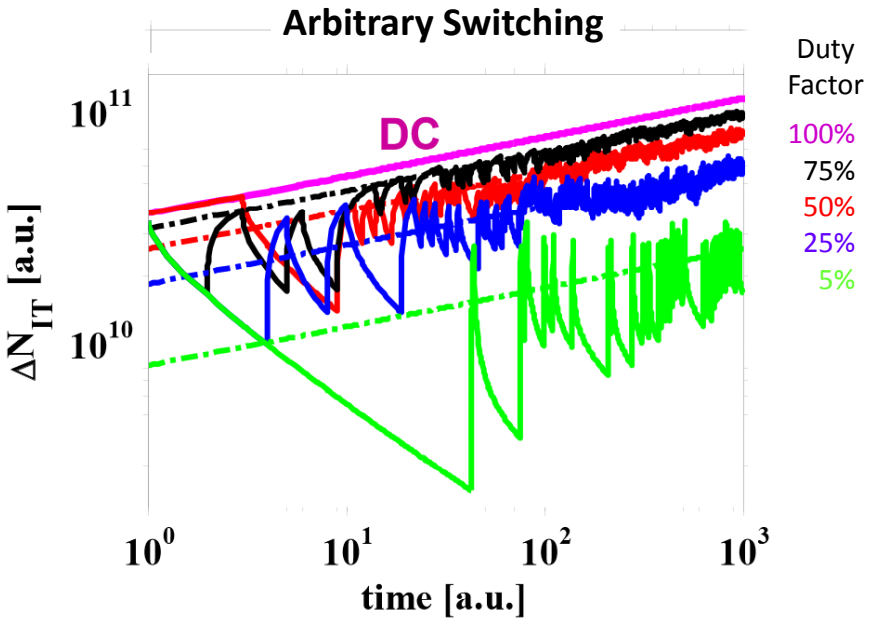
BTI: Stress vs. Relaxation

- Partial healing during relaxation leads to delay degradation that is state dependent



Kyong Taek Lee, (Samsung) IEEE (2013)

BTI and Duty Cycle



Source: Haldun Kufluoglu, *"MOSFET Degradation due to Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) and its Implications for Reliability-Aware VLSI Design ,"* Purdue University (2007)

Path Rank Analysis

- Rank paths in fresh and aged design, sorted by slack
- Non-critical paths can become critical, vice versa

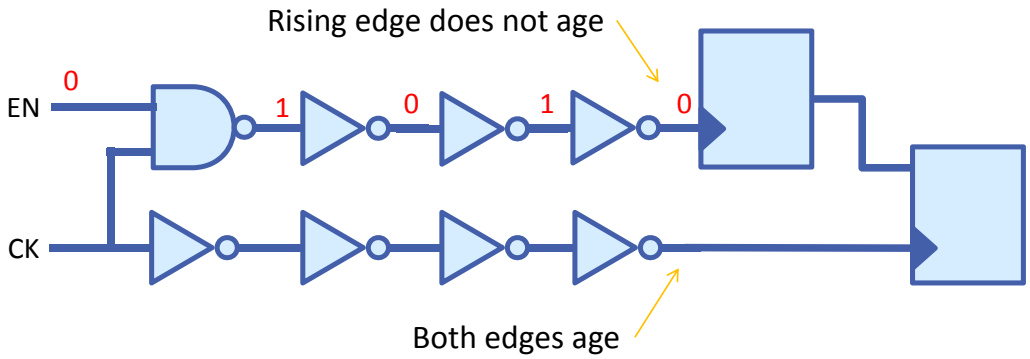
Path rank		% Timing Degradation
Fresh	Aged (Dhrystone)	
1	14084	7.64
2	9781	7.94
3	9329	8.02
4	12345	7.87
5	6220	8.31
6	36672	7.16
7	7771	8.19
8	11580	7.96
9	28975	7.40
10	20054	7.66

Path rank		% Timing Degradation
Aged (Dhrystone)	Fresh	
1	179394	15.61
2	145042	15.41
3	134419	15.18
4	1413427	17.57
5	272323	15.67
6	224034	15.46
7	331934	15.76
8	275422	15.56
9	481425	16.06
10	208561	15.24

Source: Vikas Chandra, et al. (ARM), *"Workload dependent NBTI and PBTI analysis for a sub-45nm commercial microprocessor,"* IEEE (2013)

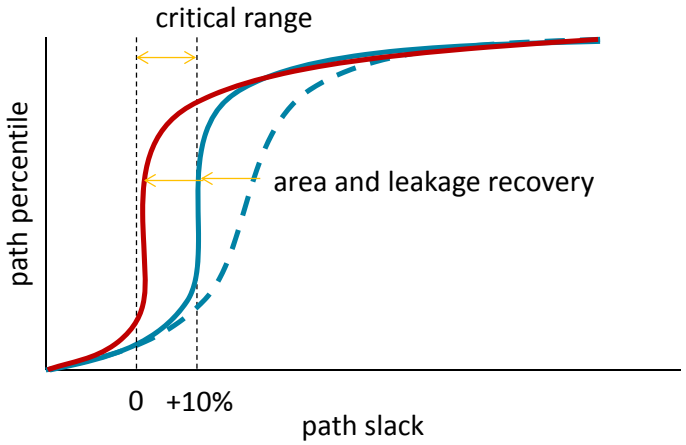
Hold Time with Gated Clocks

- Since the rising edge of a gated clock spends most of its time in recovery, it does not age
- Rising edge of un-gated clocks does age
- Leading to potential hold failures over time



Practical Advice (1/2)

- Set critical range to at least 10% of the clock period
  - Prevents area and leakage recovery from creating setup paths that will age to become critical

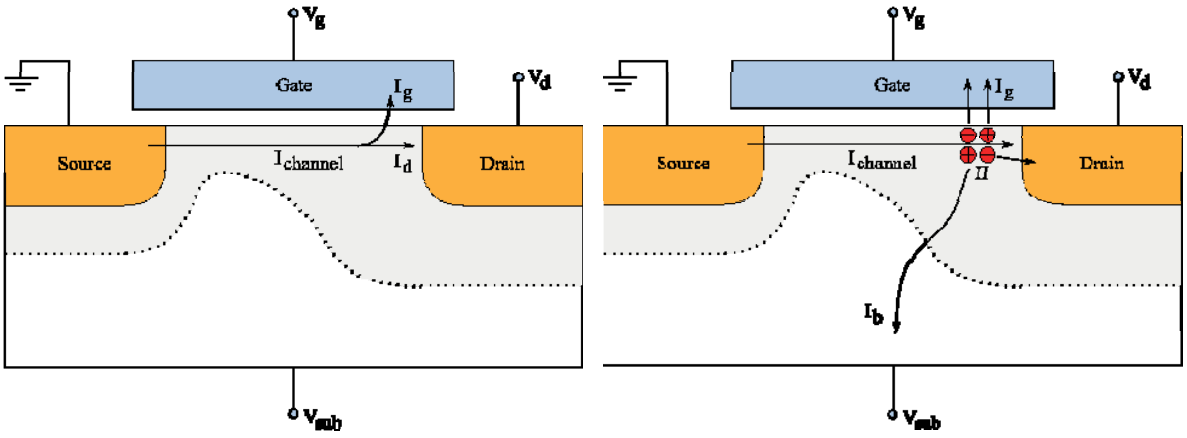


Practical Advice (2/2)

- Most gated clocks should connect directly to sequential elements
  - Identify cases of clock tree stages beyond the gated clock and add extra hold margin
- Advocate with EDA vendors for static timing with aging based on time and switching activity
  - The issue of determining an appropriate switching activity remains

Hot Carrier Injection

$$\Delta Vth \approx L_{eff}{}^{\propto} \left[t \times \frac{I_d}{W} \times \left(\frac{I_{sub}}{I_d} \right)^m \right]^n e^{\left(\frac{-Ea}{kT} \right)}$$

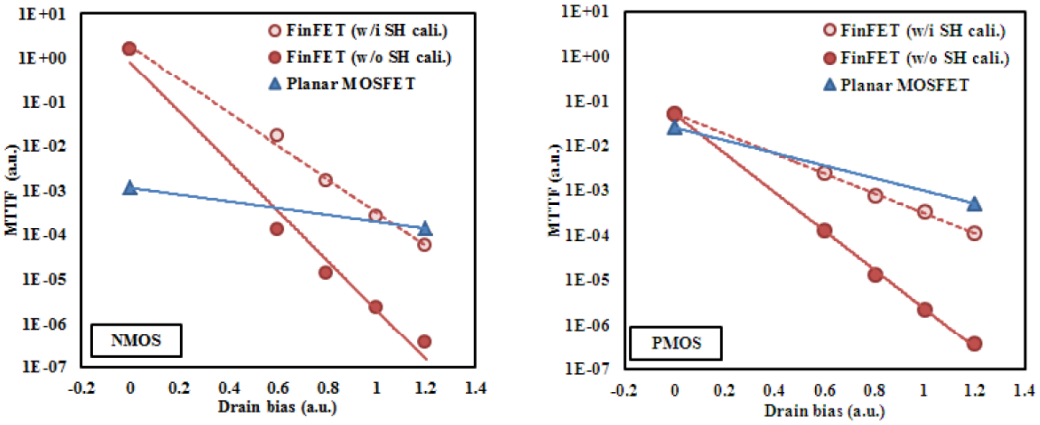


Channel Hot-Electron Injection **Drain Avalanche Hot-Carrier Injection**

Source: Robert Entner , *"Modeling and Simulation of Negative Bias Temperature Instability,"* Technische Universitat Wien (2007)

HCI: Planar vs. FinFET

- HCI in FinFET is better than planar transistors



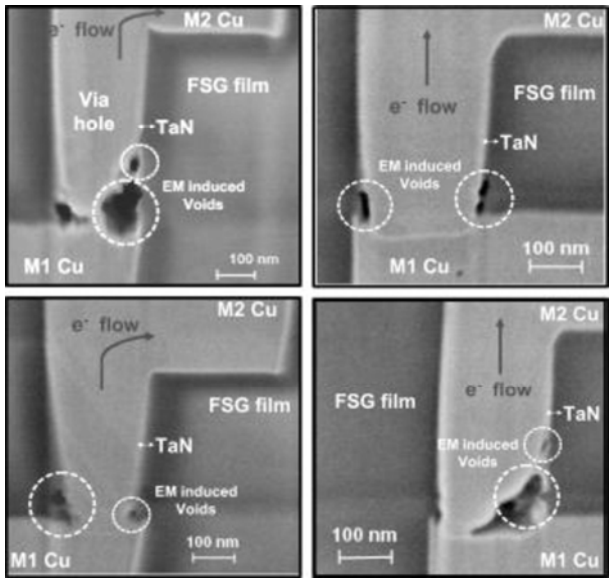
Source: S. E. Liu, et. al., (TSMC) "*Self Heating Effect in FinFETs and its Impact on Device Reliability Characterization*," IEEE (2014)

Practical Advice

- Limit the maximum transition time to reduce degradation due to HCI
  - This will insure HCI has less effect than BTI
- Advocate with EDA vendors for static timing with aging due to HCI
  - Table based on input transition, output load, and switching activity

Electromigration

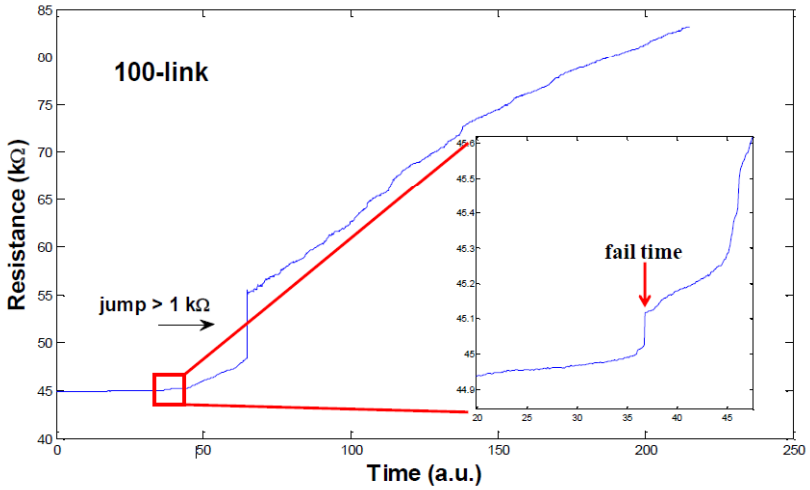
$$MTTF = Aj^{-n}e^{\left(\frac{Q}{kT}\right)}$$ (Black's Equation)



Source: Y. L. Hsu, et al., *"Failure Mechanism of Electromigration in Via Sidewall for Copper Dual Damascene Interconnection,"* ECS (2006)

EM: Resistance vs. Time

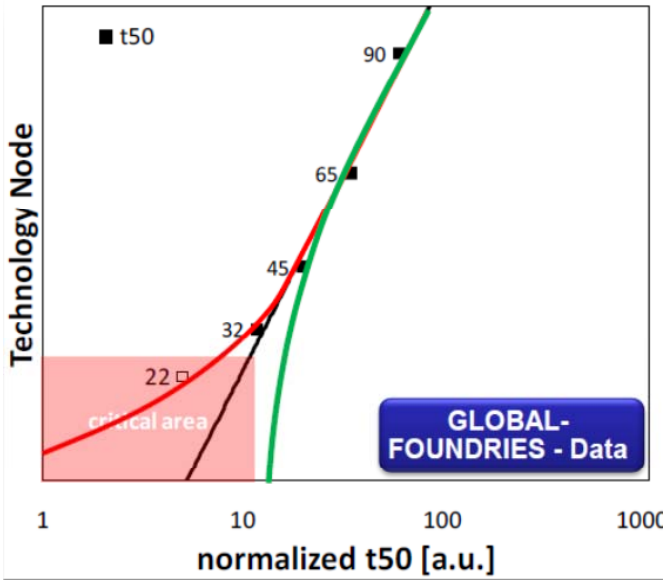
- Resistance changes as dislocations form
  - Failure criteria is specified as a given resistance shift in a percentage of samples



Source: Zhuojie Wu, *"Study of Initial Void Formation and Electron Wind Force for Scaling Effects on Electromigration in Cu Interconnects,"* University of Texas (2013)

EM Trend

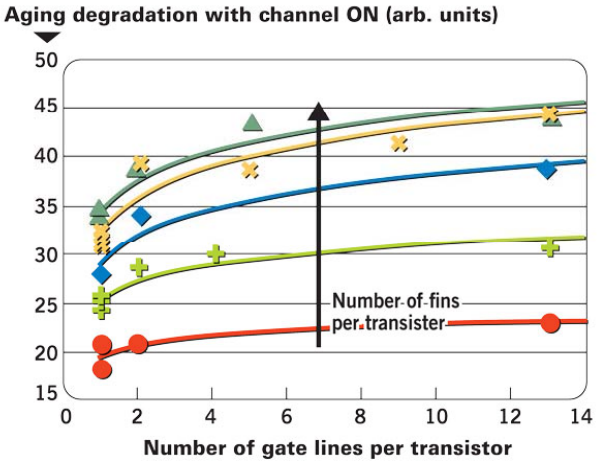
- With stronger FinFET transistors and thinner interconnect, EM is becoming critical



ITRS (2013)

EM and FinFETs

- Self-Heating in FinFETs may lead to worse EM in surrounding wires
  - Self-heat manifests as a sensitivity to the fin or gate count in switching aging degradation



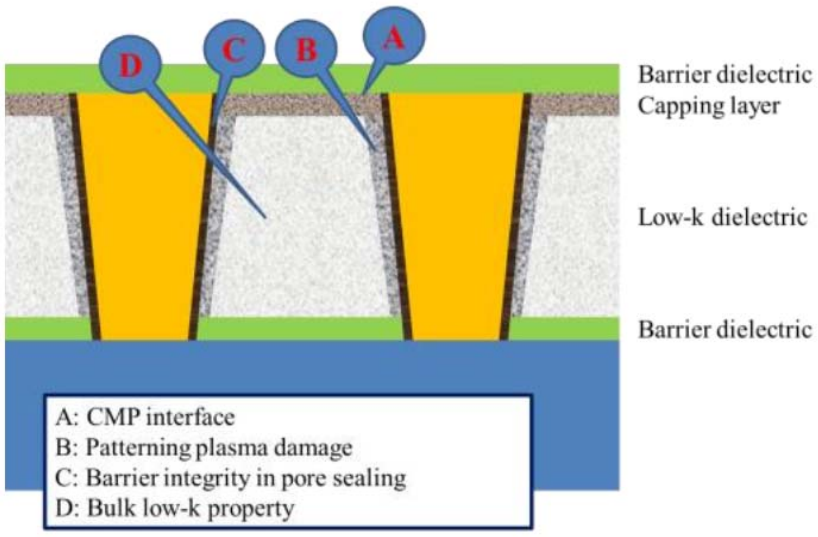
http://semimd.com/blog/tag/rram/

Practical Advice

- Take advantage of the Blech effect whenever possible, especially in VIA stacks
- Build and verify power grids early
  - Limit placement density in areas with high power
- Limit wire length and maximum transition times to reduce RMS EM violations on signals
- Follow IP provider guidelines for cell level EM compliance
- Carefully balance operating temperatures and MTBF due to EM

Time Dependent Dielectric Breakdown

$$t_{BD} = A_0 e^{-\beta V} e^{\left(\frac{-Ea}{kT}\right)}$$



Source: ITRS 2013 EDITION: INTERCONNECT

TDDB:

- Electric fields are highest at wire tips
  - Line edge roughness contributes on wire sides

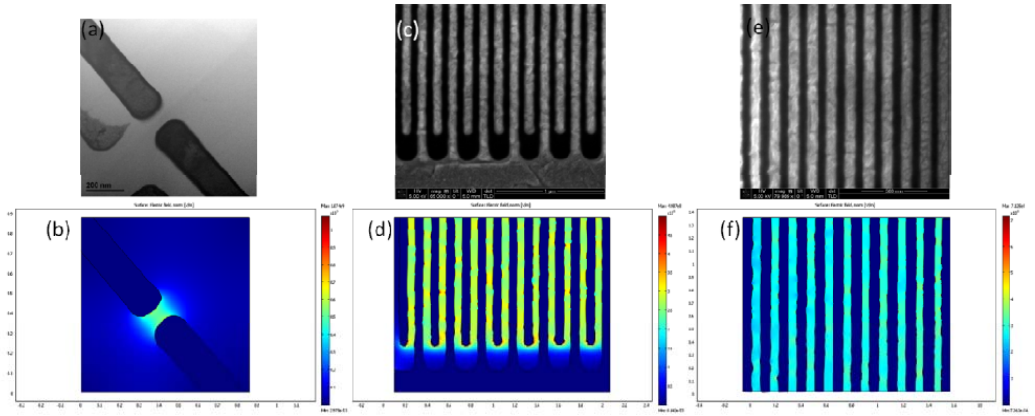
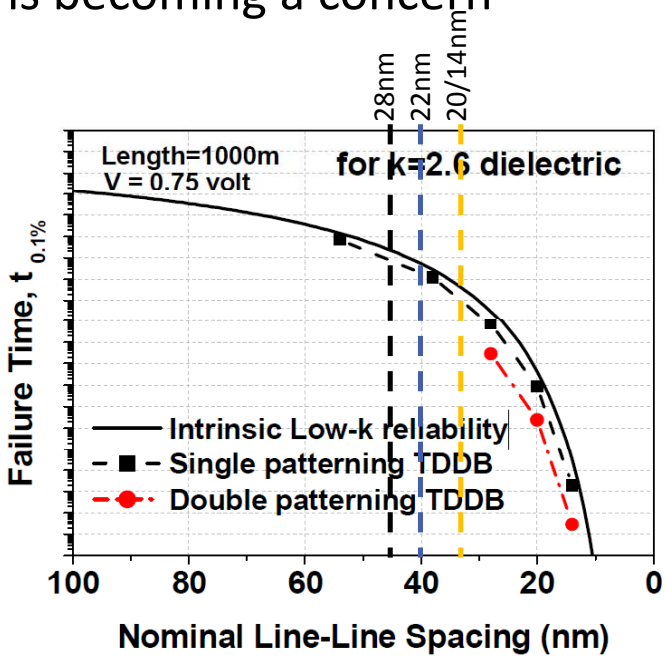


Fig.6. (a) Planar SEM view of finger test structure (b) Electric field simulation of finger test structure (c) Planar SEM view of comb structure (corner) (d) Electric field simulation of comb structure (corner) (e) Planar SEM view of comb structure (body) (f) Electric field simulation of comb structure (body)

Source: Ong, IEEE IPFA (2012)

TDDB vs. Spacing

- TDDB is becoming a concern

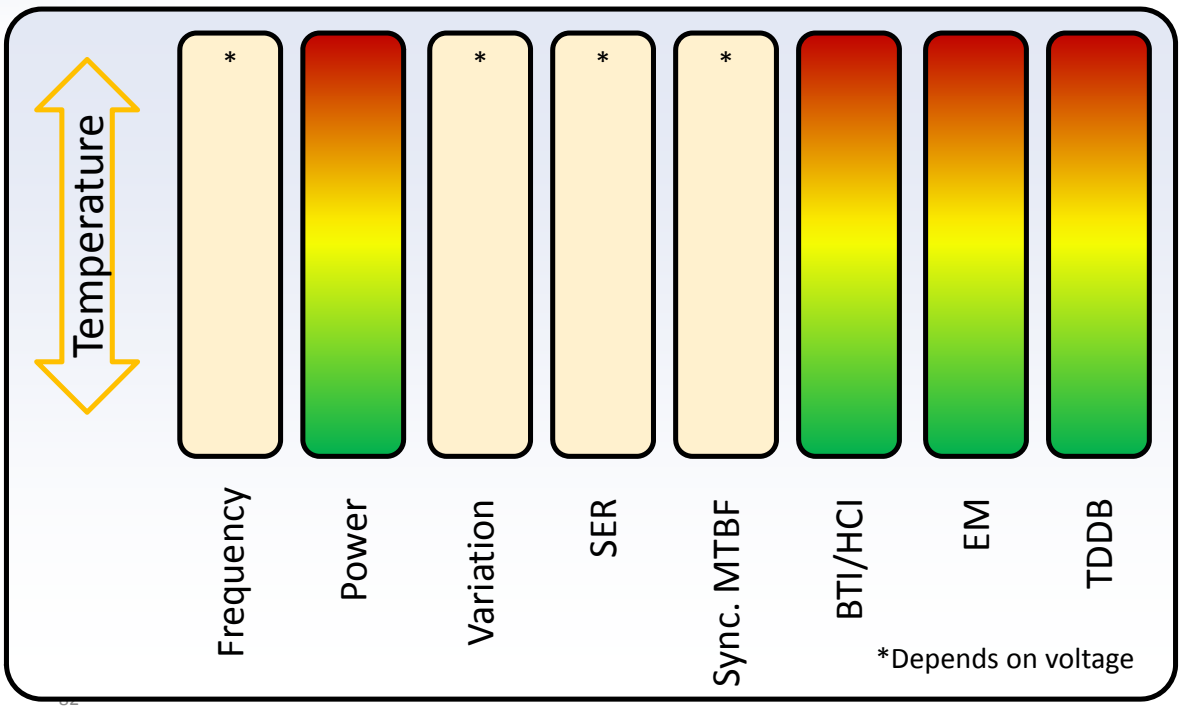


Anthony S. Oates (TSMC), *"Will Reliability Limit Moore's Law?,"* IEDM (2014)

Summary

The Balancing Act

The Balancing Act: Temperature



The Balancing Act: Voltage